

DSD LAB RECORD

Software



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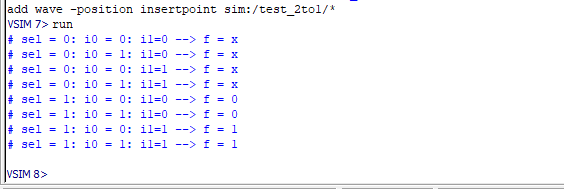
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PRAJWAN

Experiment – 1

Verification of Boolean expression

* Aim-

To verify the given Boolean expression using Model Sim software.

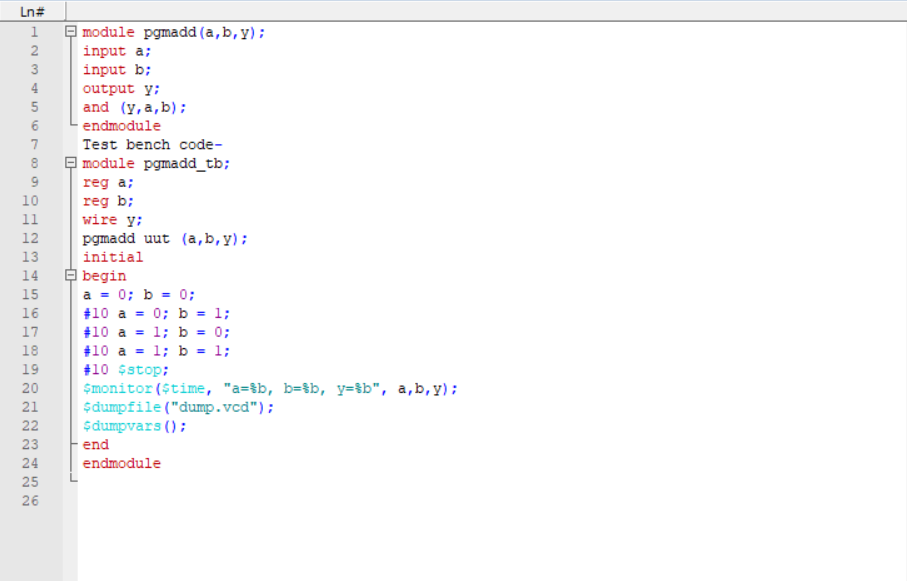
Y=AB

* Tools Required-

Model Sim software

* Code-

Design block code-



* Circuit Diagram-

A black and white diagram

AI-generated content may be incorrect.

* Truth Table-

|  |  |  |
| --- | --- | --- |
| A | B | Y |
| 0 | 0 | 0 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

* Output-

A screenshot of a computer

AI-generated content may be incorrect.

A white background with black text

AI-generated content may be incorrect.

* Result-

Hence the given Boolean expression has been verified.

Experiment – 2

Implementation of Adder and subtractor Circuits

* Aim-

To develop the source code for adders and subtractors by using VERILOG (Modelsim) and obtain the simulation.

* Tools Required- Model Sim software
* Half Adder:

i)circuit diagram:

A diagram of a circuit

AI-generated content may be incorrect.

ii)code:

Design block -

A screenshot of a computer program

AI-generated content may be incorrect.

Test bench -

A screenshot of a computer program

AI-generated content may be incorrect.

iii)Output:

A screenshot of a computer

AI-generated content may be incorrect.

* Half Subtractor:

i)Circuit diagram:

A diagram of a circuit

AI-generated content may be incorrect.

ii)code:

Design block-

A screenshot of a computer program

AI-generated content may be incorrect.

Test bench-

A screenshot of a computer program

AI-generated content may be incorrect.

iii)Output:

A screenshot of a computer

AI-generated content may be incorrect.

* Full adder:

i)circuit diagram:

A diagram of a circuit

AI-generated content may be incorrect.

ii)code:

Design block-

A screenshot of a computer program

AI-generated content may be incorrect.

Test bench-

A screenshot of a computer

AI-generated content may be incorrect.

iii)Output:

A screenshot of a computer

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* Full subtractor:

i)circuit diagram:

A diagram of a circuit

AI-generated content may be incorrect.

iii)code:

Design block-

A screenshot of a computer program

AI-generated content may be incorrect.

Test bench-

A screenshot of a computer program

AI-generated content may be incorrect.

iii)Output:

A screenshot of a computer

AI-generated content may be incorrect.

* Result-

Hence the adders and subtractors have been implemented

Experiment – 3

Design of Decoders

* Aim:

To design and implement Decoder circuit using VERILOG(Modelsim) and obtain the simulation.

* Tools Required: Model Sim Software.

2:4 Decoder:

i)Circuit Diagram:

A diagram of a circuit

AI-generated content may be incorrect.

ii)Code:

A screenshot of a computer program

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Data Flow:

A screenshot of a computer program

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Behavioural modelling:

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Test Bench:

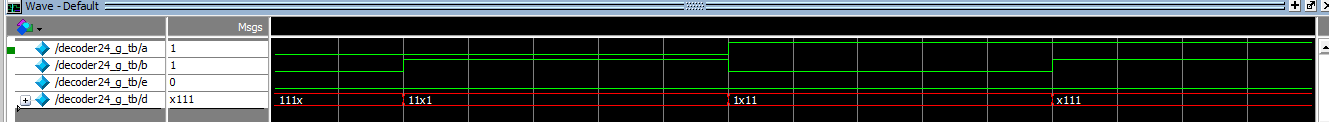
A screenshot of a computer program

AI-generated content may be incorrect.

iii)Truth Table:

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| A1 | A0 | Y0 | Y1 | Y2 | Y3 |
| 0 | 0 | D | 0 | 0 | 0 |
| 0 | 1 | 0 | D | 0 | 0 |
| 1 | 0 | 0 | 0 | D | 0 |
| 1 | 1 | 0 | 0 | 0 | D |

* Output:



A screenshot of a computer code

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* Result:

Hence decoder is designed.

Experiment – 4

Design and Implementation of Multiplexers

* AIM:

To verify and study the truth table of 2:1 multiplexer circuit using modelism

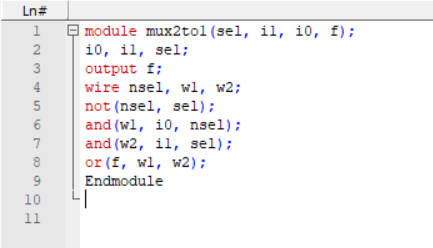
* SOFTWARE REQUIRED: MODELISM
* CIRCUIT DIAGRAM:

A black and white outline of two connected objects

AI-generated content may be incorrect.

* CODE:

GATE LEVEL MODELING:



TEST BENCH:

A screenshot of a computer program

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DATA FLOW: module mux2to1

A screen shot of a computer

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A screenshot of a computer

AI-generated content may be incorrect.

TRUTH TABLE:

|  |  |  |  |
| --- | --- | --- | --- |
| SELECT(S) | INPUT(A) | INPUT(B) | OUTPUT(F) |
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 1 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 0 |
| 1 | 1 | 1 | 1 |

* RESULT: The multiplexer was successfully designed and implemented in ModelSim using basic logic gates, and its functionality was verified with the truth table.

Experiment – 5

1(Bit) magnitude comparator

* Aim- To verify the 1(Bit) magnitude comparator using Modelsim software.
* Tools required- Modelsim software
* Circuit Diagram-

A diagram of a circuit

AI-generated content may be incorrect.

* Code-

Design block code-

A screenshot of a computer program

AI-generated content may be incorrect.

Test bench-

A screenshot of a computer program

AI-generated content may be incorrect.

* Truth Table-

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| A | B | A>B | A=B | A<B |
| 0 | 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 0 | 0 |
| 1 | 1 | 0 | 1 | 0 |

* Output-

A screenshot of a computer

AI-generated content may be incorrect.

* Result-

Thus the 1(Bit) magnitude comparator has been verified.